

## TEXTURE PROCESS MONITORING IN SOLAR CELL MANUFACTURING USING OPTICAL METROLOGY

Vamsi Velidandla<sup>1</sup>, Jim Xu<sup>1</sup>, Zhen Hou<sup>1</sup>, Kapila Wijekoon<sup>2</sup> and David Tanner<sup>2</sup>

<sup>1</sup> Zeta Instruments, 1909 Concourse Drive, San Jose, CA 95120, USA

<sup>2</sup> Applied Materials, 3535 Garrett Drive, Santa Clara, CA 95054, USA

### ABSTRACT

A novel optical metrology technique has been developed to study textured silicon wafers used to manufacture solar cells. This high efficiency optical design to maximize the signal from surfaces with reflectivity well below 1% was developed. Pyramid dimensions were measured on as sawed p-type Czochralski wafers having a bulk resistivity of 1-5 Ohm-cm. These wafers were subjected to a single step texturization process by using a non-alcoholic chemical etching formulation. Results were compared with SEM imaging. Reflectivity tests and pyramid height measurements were used to study the efficiency of the texturing processes. In a related study [2] it was found that 20µm of material removal was required to attain minimum surface reflectivity. Further removal of material affected pyramid dimensions, but did not improve surface reflectivity.

### INTRODUCTION

A fundamental property of crystalline Silicon based solar cells is their ability to minimize reflection losses via multiple internal reflections on their textured surface. Texturing is therefore one of the most important steps in the solar cell production process. On mono-crystalline Silicon wafers, the texture is realized in the form of 4-sided pyramidal structures that have a 100 base plane and are etched in the 111 plane. Current production lines have a typical pyramid dimension of 3 – 8 µm. The coarse nature of the resulting surface roughness makes it difficult to measure surface topography with contact based profilers and its highly absorptive nature makes it a challenging problem for non-contact optical metrology techniques. Solar cell manufacturers producing thousands of wafers per hour also need to balance the throughput and the economics of metrology with their process control requirements. Given that the cost of a typical silicon substrate is almost 50% of the solar cell production process, it is important to optimize the wafer thickness and texture process using proper metrology. In this paper we present a novel optical profiler solution for measuring surface texture on solar cell wafers. A high efficiency optical design to maximize the signal from surfaces with reflectivity well below 1% was developed. This enabled the inspection of bare as well Si<sub>3</sub>N<sub>4</sub> coated wafers that

were put through various stress test process conditions, such as etch bath life, etching time, and additives, to yield a wide range of pyramid sizes. Results were compared with SEM imaging of selected samples. The efficiency of texturization was monitored by measuring the surface reflection as well as pyramid heights. In this paper we present a detailed description of random pyramid characterization and corresponding reflectivity values and their effect on solar cell efficiency. In particular we show that newly developed optical metrology method as a versatile production monitoring tool for the solar cell manufacturing line

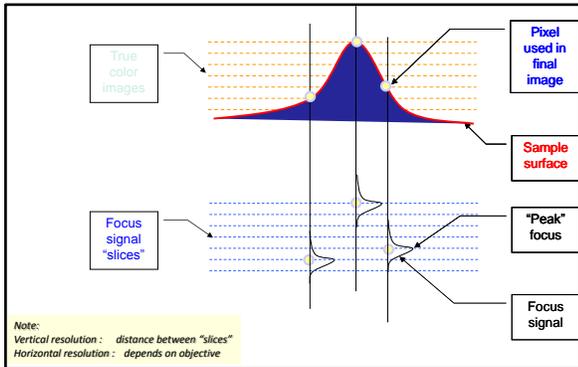
### EXPERIMENTAL

The Zeta-20 3D imaging and metrology microscope (Figure 1) was used to acquire the pyramid height data presented in this study. This vertical scanning microscope generates 3D images of surfaces by acquiring a series of images at various heights, typically a few nanometers apart.



**Figure 1 The Zeta-20 3D imaging and metrology microscope**

At each height, the points on the surface that are in best focus are detected and their height and color is stored to recreate the final true color 3D image (Figure 2). Unlike typical scanning microscopes that are limited by the depth of focus of the objective lens, the Zeta microscope uses a unique optical design that enables a height resolution that is smaller than the depth of focus.

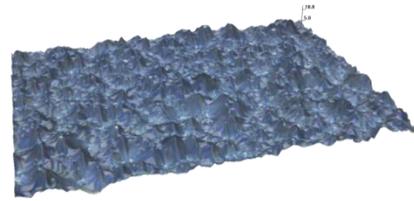


**Figure 2 Vertical Scanning and Image Generation process on a Zeta-20 optical profiler.**

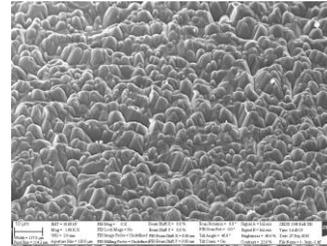
The tool used in this study has a stage resolution of 2nm and a minimum step height resolution of 70nm. Given that the measured features are of the order of 3 microns in height, this resolution was deemed enough for the pyramid dimension measurements. An additional Zeta-20 tool with a 10nm step height resolution was available (but not used in this study). In order to best characterize the pyramids on the etched silicon and nitride coated wafers, a dedicated analysis software was developed to automatically calculate the surface roughness, pyramid base dimension as well as pyramid heights. Reflectivity measurements of the textured wafers were made with a Perkin Elmer spectrometer containing a hemispherical detector. As-sawed wafers with a nominal thickness of 200 $\mu$ m were used in this study. All textured wafers were processed to complete solar cells by the Applied Materials baseline integration process flow (with POCl doping, PSG etch, passivation, screen printing, firing and laser edge isolation). Measurements of surface reflectivity and minority carrier lifetimes were made for each group of wafers. This enabled the correlation of pyramid height and size measurements to the end solar cell performance.

## RESULTS

A select group of wafers was put through various process conditions. A control group of wafers was left intact after texturing, while a sub-group was coated with Silicon Nitride (Si<sub>3</sub>N<sub>4</sub>). 3D images of the surface texture were acquired using the Zeta-20. Figure 3 shows one such wafer as imaged with the Zeta-20 as well as the SEM (scanning electron microscope). On the Zeta-20, an optical magnification of approximately 3000X was achieved by combining a 100X objective with a 0.5X coupling lens and a color CCD camera with 1024X768 pixels.



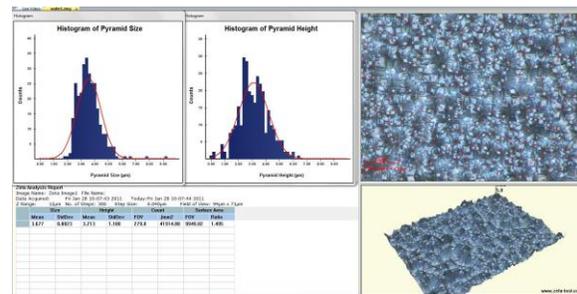
(3a)



(3b)

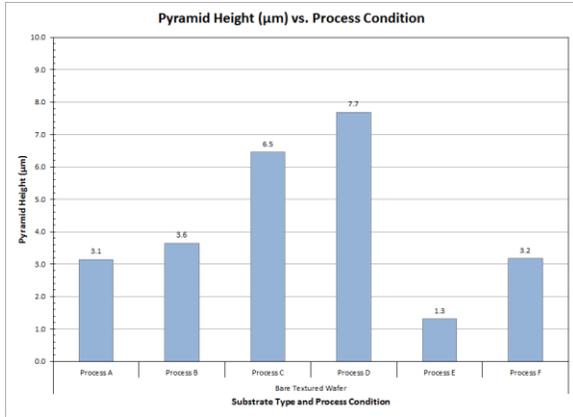
**Figure 3 Textured silicon surface as imaged with the Zeta-20 (3a) compared with an SEM image (3b).**

The images were then analyzed with the solar pyramid analysis software. The software automatically detects individual pyramids and measures the height of each peak. The mean distance between all the pyramids detected in the field of view is used to calculate the nominal pyramid size. Figure 4 shows a typical output of the Zeta 3D pyramid dimension measurement software. A histogram of the m

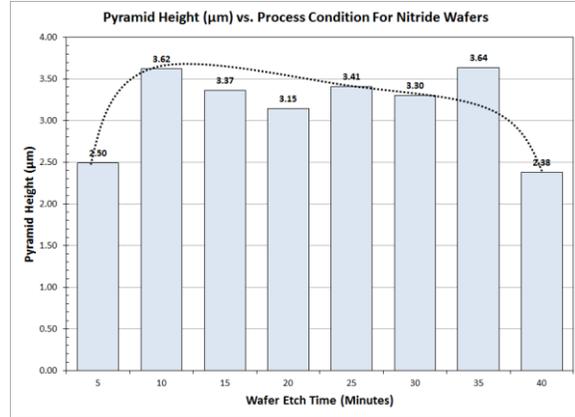


**Figure 4 Output of the solar pyramid analysis software showing the detected peaks on the top right and the histogram pyramid size and height distribution for the given field of view.**

The effect of varying process conditions is shown in Figure 5. The wafers were subjected to a varying etch bath life, etching time and additives. The effect of varying etch bath life and etching time is seen in the first four wafers, where the pyramid size increases with exposure time. The effect of additives is seen in the last two wafers wherein the additives play a key role in the pyramid size.



**Figure 5** Variation of pyramid height on textured silicon wafers when subjected to varying process conditions.



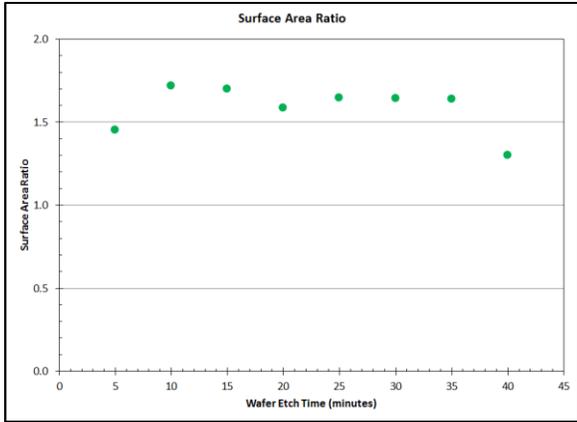
**Figure 6** Variation of pyramid height on textured silicon wafers when subjected to varying etch time.

Figure 6 shows the effect of etch time on the pyramid height distribution and Table 1 shows the measured height data. From the final solar cell performance it was determined that optimal etch time was around 20 minutes. At 5 minutes etch time, surface pyramids are formed, but the surface damage from the wire saw has not been completely removed. The pyramids are not at the optimal size. At around 20 minutes, the pyramid size is optimal and the surface has minimal reflectivity. As the etch time increases, the pyramid height essentially remains in the same range as the surface gets covered further with smaller pyramids which don't essentially change the average height. However, at extreme etch times, when the entire surface is covered with pyramids, the average height of the pyramids is drastically reduced, since there is a larger number of smaller micro-pyramids covering the surface. Further studies are planned to evaluate the outlier at 35 minutes of etch time. It is expected that the average pyramid height should first increase until 10-15 minutes of etch time and then it should decrease as the etch time increases beyond 15-20 minutes. Around 10 minutes the surface damage from the wafer saw is removed, but the surface is not fully covered with pyramids. Optimal pyramid coverage of the wafer surface is achieved around 20 minutes.

| Automated Analysis of Pyramid Height |           |                     |         |      |      |
|--------------------------------------|-----------|---------------------|---------|------|------|
| Substrate Type                       | Etch Time | Pyramid Height (µm) | Std Dev | Min  | Max  |
| Nitride                              | 5         | 2.50                | 0.84    | 0.70 | 4.80 |
|                                      | 10        | 3.62                | 1.30    | 0.50 | 6.80 |
|                                      | 15        | 3.37                | 0.97    | 1.20 | 5.60 |
|                                      | 20        | 3.15                | 1.04    | 0.80 | 5.20 |
|                                      | 25        | 3.41                | 1.23    | 1.00 | 6.40 |
|                                      | 30        | 3.30                | 1.18    | 0.70 | 5.50 |
|                                      | 35        | 3.64                | 1.33    | 0.80 | 6.60 |
|                                      | 40        | 2.38                | 0.71    | 0.50 | 3.80 |

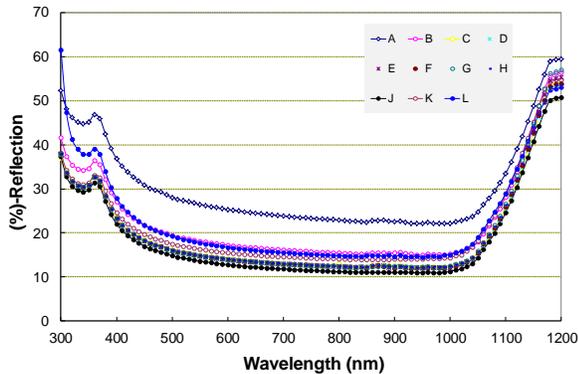
**Table 1** Variation of pyramid height on textured silicon wafers.

The measurement of pyramid height enables the calculation of an average pyramid size as well as the Surface Area Ratio for the area inspected by the Zeta-20. As can be seen from Figure 7, the surface area ratio is also optimal in the 15 to 20 minute etch time range, where the end solar cell performance is the best. As the etch time goes up and the surface is covered with smaller pyramids, the surface area ratio actually decreases. This is a very interesting phenomenon and the fact that the surface area ratio can be monitored and correlated to end solar cell performance gives the solar industry a powerful tool to optimize their process conditions and optimize yield in their production lines.



**Figure 7** Variation of effective surface area ratio on textured silicon wafers when subjected to varying etch time.

Comprehensive reflectivity measurements (Figure 8) were made on all the wafers [2]. These measurements can be correlated with the measured pyramid dimensions and the process conditions to optimize the solar cell manufacturing process and improve the end module efficiency.



**Figure 8** Reflectivity measurements on textured silicon wafers subjected to various process conditions.

### CONCLUSION

A new cost effective optical metrology method has been developed to monitor pyramid dimensions on textured silicon wafers. This non-contact technique is fast (typical scan time 40 seconds) and correlates well with the results obtained using a SEM as well as the end solar cell performance parameters. The inspection method is sensitive enough to be used either as a production monitor or as a process development tool. It was found that the pyramid height first increases as the wafer is etched and more of the wafer surface is covered with pyramids. The average pyramid height starts decreasing once the wafer surface is fully covered with pyramids and further etching creates the smaller micro-pyramids on top on the existing pyramids. This new technique can also be used to calculate the effective surface area ratio of a textured

wafer. As can be seen from the data acquired, optimal surface area ratio is achieved in the range where the surface reflectivity of the wafer is the lowest. Over etching decreases the surface area ratio parameter. The results presented in this paper validate the optical technique developed for textured wafer characterization.

### REFERENCES

- [1] K. Wijekoon et al., "Production Ready Novel Texture Etching Process for Fabrication of Single Crystalline Silicon Solar Cells", 35<sup>th</sup> IEEE PVSC, 2010, pp 3635 - 3641
- [2] K. Wijekoon et al., "Direct Texturization of as Sawed Mono-crystalline Silicon Solar Wafers: Solar Cell Efficiency as a Function of Total Silicon Removal", 37<sup>th</sup> IEEE PVSC, Seattle, 2011
- [3] P. Campbell, M. A. Green, J. Appl. Phys. 62, 243, 1987
- [4] B. L. Sopori, Sol. Cells, 25, 15, 1988
- [5] J. D. Hilton et al., Progress in Photovoltaic Research and Applications, 4, 435, 1996